

FabTime® Newsletter

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Information

Publisher: Acquired by INFICON in early 2024, FabTime has been helping fabs with cycle time and performance improvement since 1999. FabTime's [flexible reporting software](#), [cycle time management course](#), and this newsletter are now part of the INFICON [Intelligent Manufacturing Systems](#) (IMS) group.

Editor: Jennifer Robinson, Cycle Time Evangelist for INFICON

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Keywords: Yield improvement; cycle time tradeoffs; time constraints between process steps; tool dedication; advanced packaging

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Welcome

Welcome to Vol. 26, No. 5 of the FabTime Cycle Time Newsletter. I hope you're having a wonderful holiday season and wish you joy in 2026. Today's main article continues the discussion on tradeoffs in fab management, focusing on things fabs do to improve yield that may increase cycle time. We also have subscriber discussion about automated optical inspection and announcements about the new version of FabTime, the SEMI Smart Manufacturing Global Executive Committee, and advanced packaging.

Thanks for reading! – Jennifer

Community News/Announcements

In this month's community announcements, we are delighted to announce the updated version of our FabTime reporting software, as well as the appointment of INFICON's John Behnke as Co-Chair of the SEMI Smart Manufacturing Global Executive Committee. To suggest announcements, please [reach out to Jennifer via this form](#).

New FabTime version 2509 released

FabTime version 2509.0.0 was released on September 30, 2025. It is running on our demonstration server and is available for installation at customer sites. Users can now:

1. **Color boxplots by a third variable** to identify causal/correlated factors. A statistical analysis is available to suggest useful "color-by" variables. In the example below, we see boxplots of UPH by tool colored by product, revealing a bi-modal distribution by product for Stepper 02.



2. **Receive better answers from AskJen™**, which now searches past FabTime newsletters and help articles. For example, the response below draws from the help page for a metric called Earned Plan Hours. The new system also includes footnotes and suggested follow-up questions, making the answers generally more useful.

How do I interpret FabTime's earned plan hour metric?

Interpreting FabTime's Earned Plan Hour Metric

The Earned Plan Hours (EPH) metric is a measure used by FabTime software to track production activity in semiconductor manufacturing. It provides an alternative to traditional move-based metrics.

What is Earned Plan Hours?

EPH gives credit to operators when lots are tracked into tools and as processing occurs on those tools. The credit is calculated based on the planned queue time and processing time of the lot [1.0].

How is EPH Calculated?

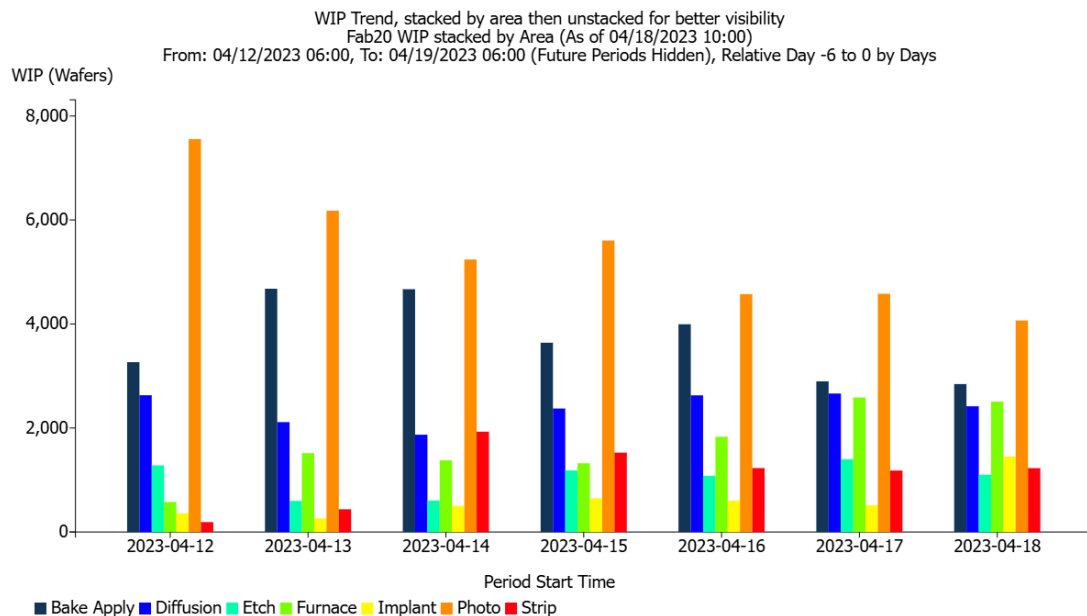
1. **Initial Credit:** When a lot is tracked into a tool, credit is given for the planned queue time of the lot at its current flow/step.
2. **Processing Credit:** As the lot is processed, additional credit is given for elapsed processing time, up to the end of the planned process time or shift change, whichever comes first.

Interpretation of EPH

- **Factory Level:** If 1,000 wafers are in the factory and being moved according to plan, each wafer should accumulate a certain number of earned plan hours during each shift (e.g., 12 hours per shift). The total EPH for the factory should be 1,000 wafers * 12 hours = 12,000 EPH. If actual EPH is greater than 12,000, the factory is ahead of plan; if less, it's falling behind.

Continue

3. **Unstack stacked charts** to get a better visual comparison. By clicking “Unstack crosstab chart” below any stacked chart and selecting “Activate” users can view data side by side instead of stacked, as in the example below. The chart shows WIP by Area. Unstacking makes the decline in Photo WIP and the rise in Implant WIP visible.



The updated version also includes:

- Security updates and bug fixes
- INFICON look-and-feel (to match other Smart Manufacturing applications)
- Improved within-application help (including the addition of recent FabTime newsletters)
- Our NexGen (d3) charting engine as the default

[Reach out to Jennifer](#) for more information or (for customers) to preview the updated version on our demonstration server.

John Behnke Named Co-Chair of SEMI Smart Manufacturing Global Executive Committee

INFICON is pleased to announce that **John Behnke**, Head of INFICON [Smart Manufacturing initiatives](#), has been appointed co-chair of the [SEMI Smart Manufacturing Global Executive Committee \(GEC\)](#). The GEC is a strategic leadership group of SEMI member companies and partners that guides industry-wide initiatives in smart manufacturing.

John is a recognized leader in semiconductor manufacturing, with extensive experience spanning process engineering, fab operations, and strategic technology leadership. At INFICON, he has been instrumental in advancing the company's Smart Manufacturing strategy, driving innovation in autonomous manufacturing, data analytics, and integrated process optimization for semiconductor fabs globally.

"John's deep industry expertise and commitment to innovation make him an exceptional choice to help lead the SEMI GEC," said **Oliver Wyrsh**, CEO, INFICON. "His appointment reflects INFICON's ongoing commitment to innovation, collaboration, and driving meaningful progress in data-driven decision-making and operational excellence in semiconductor manufacturing."

In his role as GEC co-chair, John will help guide SEMI's global Smart Manufacturing agenda, focusing on:

- Defining and advancing the Smart Manufacturing vision for the semiconductor ecosystem
- Driving collaboration across regional chapters to align global initiatives and close capability gaps
- Championing strategic priorities including Factory of the Future, Sustainability, and Future Talent development

INFICON has been a dedicated supporter of SEMI's global Smart Manufacturing Initiative, contributing expertise and leadership to advance intelligent manufacturing solutions across the semiconductor industry. Learn more in our [member success story on SEMI.org](#).

Speaking of SEMI, the next **SEMI Fab Owners Alliance (FOA) meeting**, the [Q1 Collaborative Forum](#), will be held at the Austin Marriott South in Austin, TX in February. The meeting will include a golf outing, one and a half days of case studies, and multiple evening social activities. There will also be a pre-meeting dinner and social activity for the Women of the FOA (for which Jennifer is on the governing council).

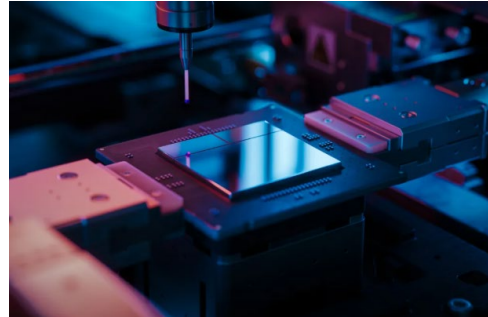


New INFICON article discusses advanced packaging in next-gen semiconductor nodes

As devices get smaller and chips become denser, manufacturers are looking for ways to continue increasing performance while minimizing power consumption and footprint. This is where advanced packaging plays a critical role. In [this new article](#) we discuss:

- Why advanced packaging matters
- The role of semi fabs in advanced packaging
- Solving the supply chain puzzle
- Integrating sensor technologies
- Meeting demands of the future

[Click here for details.](#)



Interesting Reads

Semiconductor Insights and Productivity Tips

Recent articles shared on Jennifer's LinkedIn include:

- As an IE working in the area of wafer fab scheduling, and having worked long ago in the transportation industry, I found [this WSJ article](#) fascinating. "A transit expert says (railway) travel times on the Northeast Corridor could be significantly slashed with simple fixes like smarter scheduling and faster station approaches ... for a fraction of the cost of prestige megaprojects." It makes sense to me that a complex system could see benefits from better scheduling and throughput improvement in key locations.
- An [interesting article \(also in WSJ\)](#) about how AI is helping Seagate Technology and Western Digital thanks to increased demand for (non-SSD) hard drives. "Underpinning the boost is artificial intelligence's voracious consumption of digital storage and rising prices for higher-capacity drives. In its latest financial report, Western Digital said the number of exabytes of storage it shipped—an exabyte is a billion gigabytes—rose to 190, up 32% from a year earlier. Seagate shipped 45% more of its own exabytes in the same period."
- Big news from Northrop Grumman [per Manufacturing.Net](#). Their "Microelectronics Center is now open for external aerospace and defense companies to access the company's three U.S. government-accredited semiconductor manufacturing facilities. This decision expands the secure production of defense microelectronics on U.S. soil." I agree with Vern Boyle that this is good news because it "strengthen(s) the resilience of America's semiconductor industry and supply chain," including in the area of Advanced Packaging.
- Broadcom also had [big news](#). "OpenAI plans to design its own graphics processing units, or GPUs, which will allow it to integrate what it has learned from developing powerful artificial-intelligence models into the hardware that underpins future systems. As part of the agreement announced Monday, the chips will be co-developed by OpenAI and Broadcom and deployed by the chip company starting in the second half of next year... The new agreement will be worth multiple billions of dollars."

- More [big news from Skyworks and Qorvo](#). The two companies will be combining operations “to create a U.S.-based, global leader in high-performance radio frequency (RF), analog and mixed-signal semiconductors... The combined company will strengthen its domestic production capacity and enhance its capital efficiency, supported by a robust network of supply chain partners to meet the needs of high-volume and highly specialized customers.”
- In a “highly exceptional” move, the Dutch government has [wrested control of Nexperia](#) from China's Wingtech. This follows the UK’s action in 2022 to force Nexperia to unwind their purchase of the wafer fab in Newport, Wales, now owned by Vishay, because of concerns from the US about Nexperia’s Chinese ownership. This has led to [concern within the automotive industry](#) about another chip shortage, the WSJ reports.
- An interesting report from start-up Substrate (reported in [the WSJ](#) and [The Free Press](#)) that the company plans on 1) building a compact EUV litho tool that will “produce results comparable to those of ASML’s most advanced machines” and 2) “establish(ing) a network of its own fabs (that cost in single digit billions and are) equipped with its lithography machines in time to begin producing chips at scale by 2028.” It's difficult to imagine, but I certainly wish them every success.
- And, for my fellow female industrial engineers, I was pleased to [notice in this article](#) that the newly named recipient of the Nobel Peace Prize is ... a woman who was “educated as an industrial engineer.” Those female IEs can really accomplish things!

For more industry news, [connect with Jennifer on LinkedIn](#).

Subscriber Discussion Forum

We have subscriber discussion about Automated Optical Inspection (AOI). Our main article also refers back to a prior topic with extensive discussion (cycle time and yield). If there is a topic you’ve been wondering about, [please let us know](#).

Automated Optical Inspection

A long-time friend and subscriber wrote: “One of my concerns is AOI (Automated Optical Inspection), which has been getting popular over the last ten years. These days, we use many AOI tools in our line. AOI is good for inspecting wafer surfaces. Even though AOI process times are not long, we see long queue times for our AOI steps. When we use more AOI, we may improve yield, but we hurt cycle time. I would like to see you talk about AOI in a future issue.”

Response from Jennifer: Your timing is excellent because we were planning to talk about trade-offs between cycle time and yield in this issue. We will include AOI in our discussion in the main article.

We welcome the opportunity to publish subscriber discussion questions and responses. [Submit your responses here](#).

Main Article: Choices in Fab Management: Part 2: Trading Higher Cycle Time for Higher Yield

By Jennifer Robinson

A goal in most wafer fabs is low, predictable cycle time. While there are some structural conditions in fabs that make achieving this goal difficult (high product mix, reentrant flow, time constraints), there are also **choices** that fab teams make that drive up cycle times. It's been my experience that fabs regularly trade better cycle time for three things: lower costs/higher revenue, higher yields, and what we'll call the status quo (resistance to change).

In this article, we'll discuss the second of these: choices fabs make that drive cycle times higher in the interest of improving yields. We covered choices regarding cost and cycle time in [the previous issue](#) and will cover choices regarding the status quo in the next issue. I'm sure those of you who have worked in wafer fabs for many years will have suggestions to supplement this discussion. Please [reach out to me](#) via our contact form or [on LinkedIn](#) with your suggestions.

First, some remarks on the relationship between cycle time and yield

It's straightforward to quantify the impact of higher yield on a company's bottom line. Quantifying the impact of higher cycle time is a much more complex proposition. (See [Why and How Fabs Should Focus on CT Improvement \(Issue 26.01\)](#) for a discussion of financial benefits from cycle time improvement.) What this means in practice is that where they conflict, it's more difficult to come down in favor of cycle time improvement than it is to come down in favor of yield improvement. This can be true even if a policy has a minimal impact on yield and a substantial impact on cycle time.

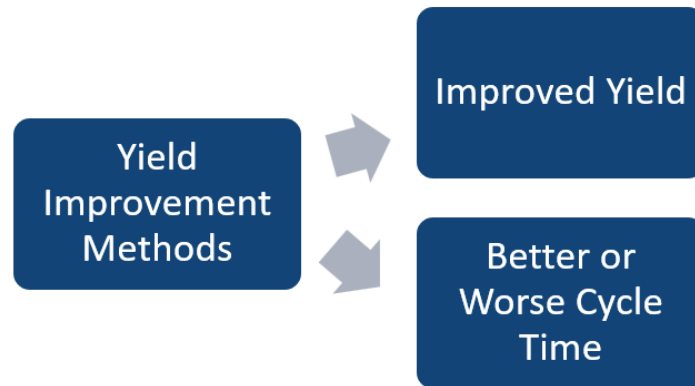
The other thing to keep in mind is that yield and cycle time are themselves related, such that improving one is likely (but not guaranteed) to improve the other. We wrote about this back in Issues 5.01 and 5.02 of the newsletter (21 years ago!). After we published our initial thoughts on the relationship between cycle time and yield (mainly that the less time wafers spend in the fab, the less opportunity there is for something to go wrong) we received a wonderful influx of subscriber feedback that helped us to revise our conclusions. You can find both issues in the FabTime Newsletter Archive. They are well worth a look, especially the Subscriber Discussion section in Issue 5.02, where nine people shared their considerable experience with the newsletter community. An updated version of the conclusions that we shared at the end of Issue 5.02 follows.

The relationship between cycle time and yield is complex and involves management trade-offs related to equipment utilization and amount of in-line testing. There may or may not be a relationship between the cycle time and yield of individual lots. Even if there is, it will tend to be difficult to quantify, because of the variability in the fab and the length of the average cycle time. Even if there isn't a direct relationship for individual lots, we, and many of the people we've talked with, believe that some relationship does exist. **We think that improving cycle time will tend to improve yields, and vice versa.** Some trends related to cycle time and yield are listed below.

- Shorter cycle time leads to increased cycles of learning, and faster yield ramp.



- Shorter cycle time may result in less opportunity for contamination, and hence higher die-per-wafer yields.
- Shorter cycle times can lead to quicker identification of yield problems, through shorter "mean time to detect" errors, and shorter in-line feedback loops.
- Better yield performance can lead to shorter cycle time through a reduction in holds and rework. That is, lots that spend considerable time on hold will tend to have longer cycle times (because of the hold time) and worse yields (because the holds are often because of yield problems to begin with) than other lots.
- Some of the techniques used to improve yield can make cycle time worse. We review four of these in the next section.



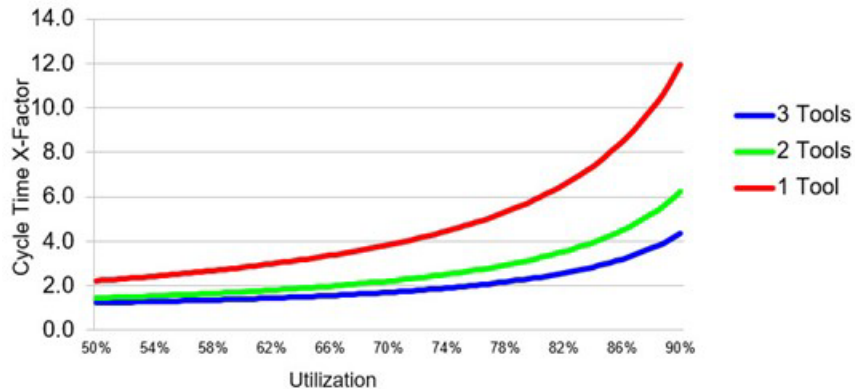
Four things that fabs do to improve yield that can also increase cycle time

Of course, not all fabs do all these things. But I'm sure that at least a few of these are familiar to many of you.

1. **Let process restrictions lead to single path operations:** A conservative approach for minimizing scrap can be to restrict processing for a given recipe to a single tool, rather than qualifying a second or third tool. Of course, this only applies to situations where the fab has multiple tools in a given tool group.
 - **Likely outcome:** Average cycle time per visit through the operation in question will be approximately double what it would be if there were two qualified tools. The reason is that when you only have one qualified tool for an operation, lots passing through the operation are subject to all the variability that occurs at that tool. If the tool goes down, all the lots wait. If there's a lot with a lengthy process time or a hot lot that jumps to the front of the queue, all the other lots are delayed. When you have two qualified tools, the probability of both of those tools being impacted at the same time by adverse events like these is significantly lower.

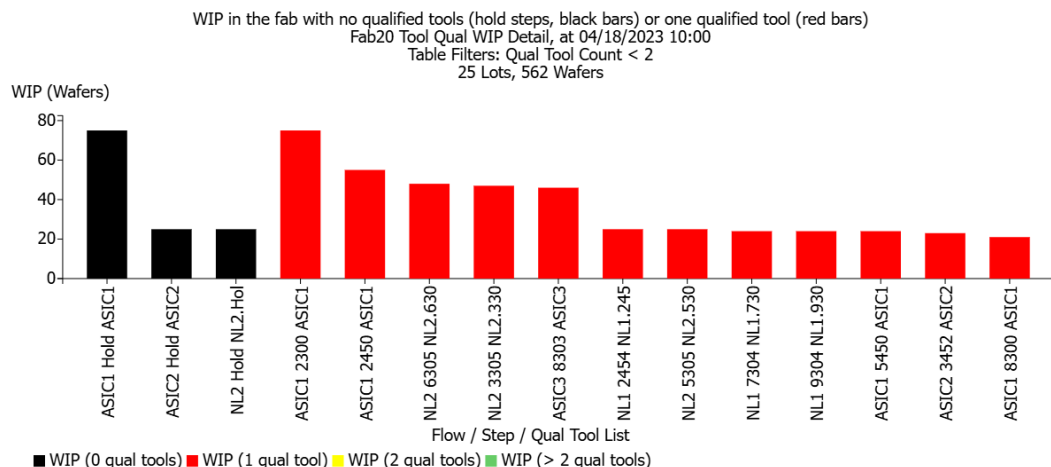
This is illustrated in the graph below, which shows the operating curve for tool groups with one, two, or three tools. At the same utilization per tool, the x-factor on the red curve (one tool) is approximately twice the x-factor on the green curve (two tools). See [The Impact of One-of-a-Kind Tools on Fab Cycle Time](https://www.inficon.com/en/fabtime-registration) for more details.

Number of Qualified Tools: Impact on Cycle Time Operating Curves



- **What you can do:** Many fabs have policies that require at least two qualified tools per operation before a new flow is released to production. We've even heard of foundries that require three qualified tools per operation. In other cases, a fab will accept single path restrictions for new low volume flows, with the intent of qualifying a second tool later, as volume rises. The trick here, of course, is to be disciplined about going back to qualify that second tool. Qualifications can also expire, resulting in a cost in time and labor to re-qualify tools. The obvious risk here is of letting the second (or even the first and only) qualification expire and not re-qualifying tools for the operation.

We recommend regularly reviewing a chart that shows the number of qualified tools for each operation, as shown below. In this example, only operations with WIP waiting are shown. However, a filter can be applied to include other operations that have WIP anywhere along their flow, even if there is no WIP at the operation right now. The point is to have systems in place that check for single path operations due to process restrictions and encourage process engineers to qualify a second tool.



INFICON is also working with one of our customers on a new qualification management product that uses optimization to help fabs intelligently manage

which tools are qualified for which product and when, based on inventory forecasts. This aligns with our recommendation from [the prior issue](#) for fabs to invest to move up the Smart Manufacturing pyramid. [Contact us](#) for more information about the new qualification management product.

2. **Do too many inspections:** If we inspect lots frequently, then we'll identify problems earlier, improving overall line yield. However, time spent doing inspections is non-value-added in terms of cycle time and also requires operator resources. Inspection tools can become constraints in some cases. It seems obvious that a point of diminishing returns exists, where additional inspections are of limited benefit in reducing scrap, but add significant cycle time.

- **Likely outcome:** When inspection steps count as moves, teams can be incentivized to over-inspect. Fabs vary in their treatment of inspection steps as moves (or completes, in FPS terminology), and in whether inspection steps “count” as part of manufacturing cycle time. They are non-value-added, in that nothing is added to the wafer, but are still under the control of the manufacturing organization (hence can be considered part of manufacturing cycle time). A lot with a higher percentage of requires inspection will generally have a longer cycle time than other lots.

A fab that is operator constrained that over-inspects may find that operators are spending time doing inspections rather than making value-added moves. This will negatively impact throughput and profitability for the fab.

Automated Optical Inspection (AOI), as mentioned in the subscriber discussion forum of this issue, raises the stakes. On the upside, AOI tools can catch defects early, creating a continuous improvement environment. AOI is non-destructive and supports advanced nodes. On the other hand, AOI tools are expensive and take up cleanroom space. High resolution scans can significantly increase cycle time. AOI tools require significant engineering overhead to make sure that the settings aren't overly sensitive (leading to false alarms). The subscriber who wrote in above captured the situation well: “Even though AOI process times are not long, we see long queue times for our AOI steps. When we use more AOI, we may improve yield, but we hurt cycle time.”

- **What you can do:** Fabs can disincentivize over-inspection by not counting inspection steps as moves. They can also measure cycle time contributed by inspection steps (including AOI steps) and analyze the historical relationship between inspection and yield rates, looking for inflection points where yield improvement levels off. Automated software products such as INFICON's [Metrology Sampling Optimizer](#) (MSO) can help here by balancing quality with risk.



The system can find the least number of lots to sample to meet the combined requests of engineers. MSO has demonstrated a 30% reduction in lots at risk.

3. **Make time constraints between process steps too tight, or too frequent:** It's common in wafer fabs to have time constraints between process steps. A lot must start processing at a later operation within some time window after completing processing at an earlier operation. A common example is a bake step that must be completed within some time window of the prior clean operation. Such constraints are also called queue time limits, time bound sequences, and time links. They are typically put in place by process engineers to improve yields in the fab. When the time windows are too tight relative to operational conditions in the fab, cycle time and capacity can be wasted, particularly if there are multiple steps inside the time constraint loop. When there are many time constraints in the fab, scheduling and dispatching are more challenging (though of course advanced scheduling software like [the INFICON Factory Scheduler](#) can help).

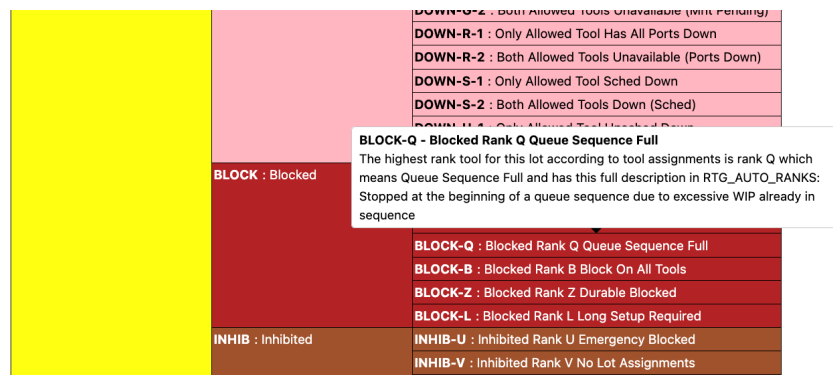
- **Likely outcome:** When a time constraint is violated, the lot must go back to the first operation in the sequence for reprocessing. When this happens, capacity is lost at tools running the first operation (increasing cycle time for all lots that use that tool), and cycle time of the reprocessed lot is increased by the reprocessing time. There is also increased variability in the arrival rate to the later operation. There can be intervening steps between the initial and final operation of a time constraint loop. These multi-step systems are particularly difficult to manage. Even a system involving two steps holds considerable complexity.

Another outcome that can happen in the presence of time constraints is that operations teams are so determined not to violate them that they hold WIP outside of the time constraint loop until the downstream tool is available. Unless carefully managed, this can inflate queue time at the upstream tool, and waste capacity on the downstream tool.

- **What you can do:** Time constraints between process steps are a hidden source of cycle time that is directly driven by yield improvement goals. The thing to do then, to better manage this trade-off, is make the cost in terms of cycle time more visible. Exactly how you do this will depend on your fab MES and how you log transactions. One idea is to add a rework code that includes "violated time constraint," so that you can filter for move transactions matching that code. Then you'll know how frequently lots are reprocessed at a given tool or operation.

A clue to the more subtle issue of people holding lots upstream waiting for the downstream tool to be available is significant Standby-WIP-Waiting time on the first tool in the time constraint loop. Logging the tool to a sub-state like "waiting for time constraint loop to clear" would allow filtering to view this data.

Alternatively, you could have a WIP state like "waiting to enter time constraint loop" as a subset of queue time. In INFICON's Enhanced Cycle Time (ECT) state model, we have a state called Block-Q, or Blocked Rank Q Sequence Full, that captures the fact that the lot is "Stopped at the beginning of a queue sequence due to excessive WIP already in sequence." This state will be displayed in future versions of FabTime and can be used to make the cost of such time constraints more visible.



You can find recommendations for minimizing time constraint expiration in this article: [Managing Time Constraints between Process Steps in Wafer Fabs \(Issue 24.02\)](#).

4. **Tie future holds to a specific engineer, turning process engineers into effective one-of-a-kind tools:** Every fab that I know of uses future holds. Future holds are situations where an engineer specifies that a lot will go on hold at some future step, so that the engineer can check something. Future holds can help with yield because the engineer identifies ahead of time where there might be a problem and plans an appropriate intervention. The problem with future holds, however, is that they are frequently tied to a specific engineer. That engineer might be unavailable at the time that the future hold comes due.

- **Likely outcome:** Future holds generally inflate the cycle time of the lot in question. Most fabs run 168 hours a week, 50-52 weeks a year. That's 8400 to 8736 hours a year (not counting leap day). Process engineers are people. They go home at night. They take vacations. Sometimes they're out sick. They're onsite for something like 25% of the time that the fab is running. (Even if it feels like more than that.) And even when they're there, they are usually busy with other things. What this means is that when you have a future hold for a specific engineer, there is an excellent chance that when the future hold comes due, that engineer will not be available. This leads to increased cycle time.
- **What you can do:** The obvious thing to do here, just like with the single path operations, is to make a backup available. Every future hold should have a primary and a secondary engineer (who ideally doesn't work on the same shift). Alternatively, some sort of team structure should be set up, like a call schedule for doctors, where someone is responsible for triaging the future holds when they come due. What makes sense for a given fab will depend on that fab's situation. (How many engineers are there? How frequent are the future holds?) The important thing is not to create situations where your process engineers act like one-of-a-kind tools.

In our [FabTime reporting software](#), engineers can set up automated alerts for future holds. ("Notify me when Lot XYZ reaches Step ABC.") When triggered, the alert automatically goes to the email address of the person who created the alert. However, that person can also send the alert to another email address, which could be a team address. We highly recommend this practice. An example is shown below.

Edit existing Lot alert

Save Changes

Cancel

TO jennifer.robinson@fabtime.com (Alerts are always sent to your email address.)

CC Engineering1@FabTime.com

SUBJECT There's a future hold for this lot. Notify me and notify Engineering1 as backup.

SEND IF Lot #1831

Opn Queue (Hours)



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DURING Select a shift.

BETWEEN start time hh:mm and end time hh:mm (Use a 24-hour clock, e.g. enter 3:30pm as 15:30.)

SLEEP 1 hours after sending an alert.

Save Changes

Cancel

Conclusions

The interaction between cost and cycle time, as outlined in the [first article of this series](#), is predictable (non-linear, but predictable). You can spend money (on tools, staff, or software tools) to reduce cycle time. Being more frugal about such spending is likely to increase cycle time. With cycle time and yield, the relationship is more complex. While reducing cycle time will tend to improve yield (through faster identification of defects and shorter learning cycles), the impact of yield improvement efforts on cycle time is more mixed.

More restrictive tool qualification tends to reduce scrap. But we know that cycle time is much higher through single path operations. More frequent inspections allow quicker problem detection and improve yields. Again, this is at a cost of higher cycle time. As fabs advance to Automated Optical Inspection (AOI) the problem is magnified, because the inspection tools are more expensive, and more likely to be run at a high loading that drives up queue time. Time constraints between process steps and future holds are other examples of techniques used by engineers to maximize yield that can be counterproductive for cycle time.

None of this is to say that fabs shouldn't use these yield improvement techniques, of course. But it's worth considering the tradeoff in increased cycle time, particularly given that shorter cycle times in and of themselves can help to improve yields.

Closing Questions for Subscribers

Does your fab do any of the things mentioned above? What else would you add to this list? (Any responses shared will be shared anonymously.)

Further Resources

All past FabTime newsletters are available in PDF format from the FabTime Newsletter Archive. Please [reach out to me](#) for the link or look in the most recent email issue of the newsletter. You can download individual issues or download a zip file containing all past issues. Some articles have been re-published on the INFICON website. Those are linked above where mentioned.