

# FabTime® Newsletter

Volume 26, No. 1

February 2025

## Information

**Publisher:** Acquired by INFICON in early 2024, FabTime has been helping fabs with cycle time and performance improvement since 1999. FabTime's [flexible reporting software](#), [cycle time management course](#), and this newsletter are now part of the INFICON [Intelligent Manufacturing Systems](#) (IMS) group.

**Editor:** Jennifer Robinson, Cycle Time Evangelist for INFICON

**Date:** Tuesday, February 11, 2025 – Vol. 26, No. 1

**Keywords:** Cycle Time Improvement, Factory Physics, Wafer Fab Financials, Cost of Cycle Time, Fab Management

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## Welcome

Welcome to Vol. 26, No. 1 of the FabTime Cycle Time Newsletter, the first issue sent via our new method. Our main topic is about how and why fabs should focus on cycle time improvement. We also have subscriber discussion on various topics and announcements about the upcoming FOA Collaborative Forum and the progress of our new AskJen™ AI-powered expert chat feature. Software tips will no longer be included here but will be shared with customers separately.

Thanks for reading, and Happy New Year! – Jennifer

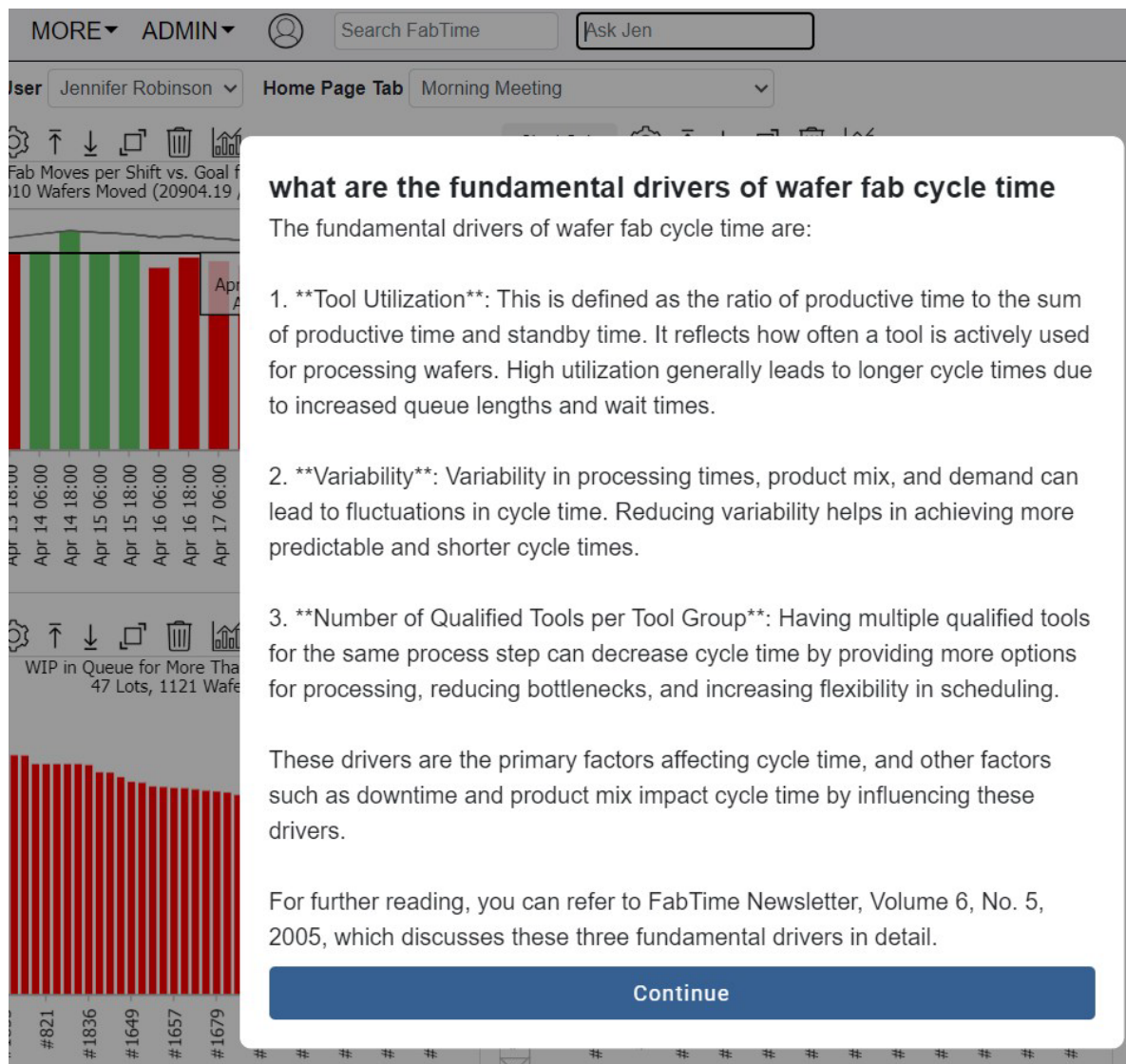
## Community News/Announcements

The INFICON team is looking forward to the upcoming FOA Collaborative Forum, to be held in Phoenix later this month. We're also pleased to offer an update on our AskJen AI-powered chat feature.

### Update on AskJen™

In the previous newsletter issue, we unveiled **AskJen**, an innovative AI-powered expert chat feature designed to provide 24/7 access to advanced insights into semiconductor operations.

AskJen harnesses cutting-edge Large Language Model (LLM) technology combined with over 25 years of FabTime cycle time management newsletter issues to empower semiconductor professionals with instant answers to operational questions.



The screenshot shows the FabTime software interface. At the top, there's a navigation bar with 'MORE', 'ADMIN', a user profile icon, a search bar labeled 'Search FabTime', and a chat input field labeled 'Ask Jen'. Below the navigation bar, the user is identified as 'Jennifer Robinson' and the current view is 'Home Page Tab' with a 'Morning Meeting' dropdown. The main content area is divided into two sections. The top section, titled 'Fab Moves per Shift vs. Goal', shows a bar chart with green bars for 'Apr 13 18:00' through 'Apr 16 18:00' and red bars for 'Apr 17 06:00' and 'Apr 17 18:00'. The bottom section, titled 'WIP in Queue for More Than 47 Lots, 1121 Wafers', shows a bar chart with red bars for various lot numbers: #821, #1836, #1649, #1657, and #1679. A chat window is overlaid on the right side of the interface. It contains the question 'what are the fundamental drivers of wafer fab cycle time' and the answer: 'The fundamental drivers of wafer fab cycle time are: 1. \*\*Tool Utilization\*\*: This is defined as the ratio of productive time to the sum of productive time and standby time. It reflects how often a tool is actively used for processing wafers. High utilization generally leads to longer cycle times due to increased queue lengths and wait times. 2. \*\*Variability\*\*: Variability in processing times, product mix, and demand can lead to fluctuations in cycle time. Reducing variability helps in achieving more predictable and shorter cycle times. 3. \*\*Number of Qualified Tools per Tool Group\*\*: Having multiple qualified tools for the same process step can decrease cycle time by providing more options for processing, reducing bottlenecks, and increasing flexibility in scheduling. These drivers are the primary factors affecting cycle time, and other factors such as downtime and product mix impact cycle time by influencing these drivers. For further reading, you can refer to FabTime Newsletter, Volume 6, No. 5, 2005, which discusses these three fundamental drivers in detail.' At the bottom of the chat window is a blue button labeled 'Continue'.

We now have AskJen running in FabTime version 2411 on our demo development server. An example is shown above. If you are an INFICON software customer and are interested in testing AskJen, please [reach out to Jennifer via this form](#).

## Upcoming FOA/WFOA events in Phoenix

The INFICON team is looking forward to participating in the upcoming [Fab Owners Alliance Collaborative Forum](#), to be held at the Wigwam Resort in Phoenix February 24-27. Jennifer will be attending the Women of the FOA dinner and social activity on Tuesday evening, as well as the general sessions on Wednesday and Thursday. She hopes to see you there!

A team from INFICON has also submitted a case study with the team from Wolfspeed in Durham.

### Improvement of Factory Digital Twin and Lot Delivery at Wolfspeed using INFICON Applications

At Wolfspeed's North Carolina Factory (NCF), managing lot transaction data was a challenge due to the use of two separate Manufacturing Execution Systems (MES). This fragmented setup made it difficult to compile and analyze factory-wide metrics across all work-in-progress (WIP). By implementing INFICON's [Digital Twin](#), NCF now consolidates all lot transaction data into a single, unified database with a consistent data structure, enabling streamlined analysis and better decision-making.

NCF also faced difficulties optimizing location tracking and lot delivery between tools located across multiple buildings. Using the centralized data from the Digital Twin, NCF also deployed the INFICON [Factory Scheduler](#) to efficiently plan when and where lots should be delivered.

Additionally, the INFICON [NextMove](#) application tracks lot locations in real-time on the factory floor and assists with delivery.

The introduction of NextMove has proven especially valuable, providing robust location tracking and clear, actionable lot delivery instructions to operators. This has improved logistics, **reduced dependency on paper travelers**, minimized handling errors, and enhanced overall operational efficiency.

In this presentation, we will outline how NCF implemented the Digital Twin, Scheduler, and NextMove. We will also discuss the significant benefits achieved, including improved data accuracy, streamlined workflows, and smoother factory operations. These advancements have not only addressed longstanding challenges but have also set the stage for sustained efficiency improvements in the future.

## Interesting Reads

### Semiconductor Insights and Productivity Tips

Recent articles shared on Jennifer's LinkedIn include:

- [An Arizona Republic article](#) about the announced closure of the Microchip wafer fab in Tempe. Jennifer notes: "I was sad to hear the news this week about the planned closing of this fab. I've enjoyed working with the team there as part of both FabTime and INFICON. Wishing all the best to the team in Tempe during this challenging time."
- A [Manufacturing.Net](#) piece about Bosch's plans and CHIPS Act funding for their Roseville, CA site. Jennifer says: "It's nice to see this older fab being transformed and (relatively) local industry jobs being kept and expanded."

"Bosch announced that it signed a preliminary memorandum of terms with the U.S. Department of Commerce to receive up to \$225 million in proposed direct funding under the CHIPS and Science Act. The proposed investment would support the development of semiconductor manufacturing in the U.S. Bosch plans to invest up to \$1.9

billion to transform its site in Roseville, California, into a facility that produces and tests silicon carbide semiconductors... The (40-year-old) Roseville site currently employs around 250 associates with potential to grow in the future.”

- A [great article in The Wall Street Journal](#) about how complex ASML EUV systems are, and how they require highly trained, 24x7 maintenance engineers. This is illustrated by a profile of a 29-year-old ASML engineer who supports the Micron fab in Boise. Jennifer says: “It’s my hope that this article inspires other young engineers to consider the semiconductor industry.”
- An [announcement](#) about onsemi acquiring the NexGen Power gallium arsenide wafer fab in New York.
- A [NY Times article](#) (login required) about how half of the employees at the new TSMC fab have been brought in from Taiwan and the impact that this influx is having on Phoenix.

“In more than a dozen interviews, Taiwanese workers, their spouses and their children said they had decided to uproot their old lives for a combination of new experiences, English education for their children and financial incentives — up to triple the usual salary along with perks like housing subsidies.”

- A nice [summary of recent Chips Act funding awards](#) in the Semiconductor Engineering Week in Review. See also [a broader summary of more than 100 notable chip industry facility/fab investments in 2024 here](#).

For more industry news, [connect with Jennifer on LinkedIn](#).

## Subscriber Discussion Forum

We’ve had subscriber discussion this month about how equipment suppliers can help fabs to maximize productivity, what tool state to use for engineering lots, and the December issue on The Waddington Effect. If there is a topic that you’ve been wondering about, [let us know](#).

### How can equipment suppliers help fabs to maximize productivity?

A [Fundamentals of Fab Cycle Time webinar attendee from an equipment supplier](#) wrote: “Do you have any models or experience working with equipment suppliers to understand how we can configure/operate tools to help fabs maximize productivity? We have done some internal work ourselves, but I wonder if there is more capability out there with collaboration to optimize the tool for fab operational efficiency (rather than over optimize unit process at the expense of fab efficiency).”

**Response from Jennifer:** I have done a special two-hour version of my [Teams-based cycle time course](#) for another equipment supplier, selecting the most relevant content from the typical four-hour class. This is more detailed and more interactive than the overview webinar that you mentioned. I also presented another webinar that focused on [metrics for mitigating the impact of equipment downtime on fab cycle time](#), which has obvious relevance for equipment suppliers. But I haven’t directly looked at collaboration between the fabs and the equipment suppliers to optimize performance.

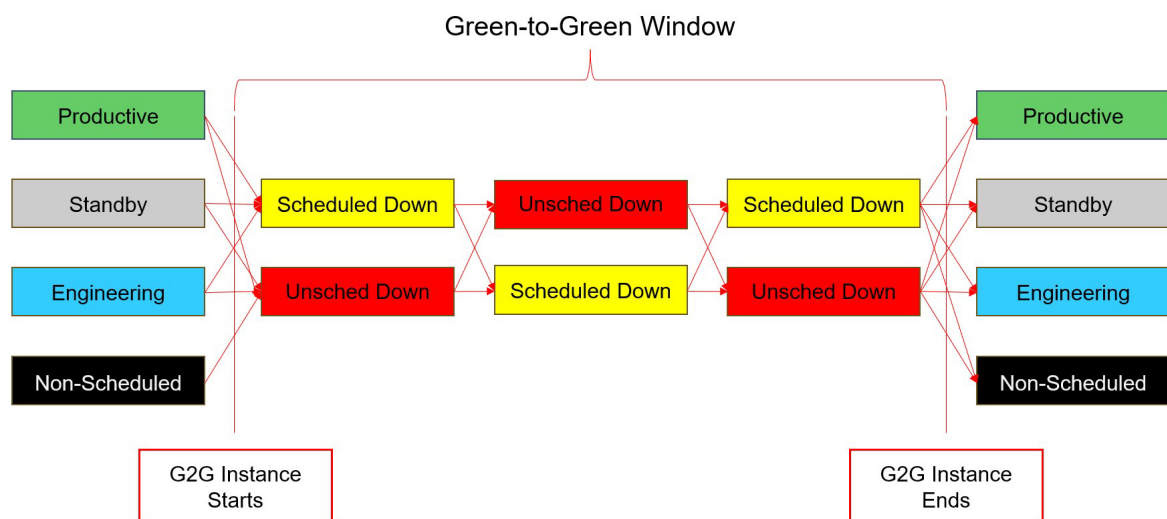
I do have a few ideas that might be helpful:

- Anything that an equipment supplier can do to make it easier to qualify additional tools for a given recipe, without sacrificing yields, would also be helpful for fab cycle time.
- To minimize the negative effect of downtime, equipment suppliers should ensure that tools have high overall availability, short down times (both scheduled and unscheduled), and low variability of availability from day to day.
- Equipment suppliers can also help fabs by reducing both the duration of and the variability of process times. Making process times more efficient (shorter) helps fabs to free up buffer capacity on the tools. Buffer capacity in turn helps protect against variability. Making process times more consistent from lot to lot reduces variability and helps bring down cycle time.
- Because of the impact of the number of qualified tools on fab cycle time, a fab will sometimes be better off having two slower tools, rather than one faster tool, especially if the reliability of the fast tool isn't good. Of course there are other things to think about here (layout, staffing, etc.), but it might be worth studying this effect at some point.

## What tool state should we use for engineering lots?

A **subscriber from a mask manufacturing factory** wrote to me after attending our equipment downtime metrics webinar: “In your Green-to-Green chart, what would you consider Engineering time? I’m having an ongoing debate with our process engineers about whether their experimental lots ought to run under green/productive time vs. engineering time. Today they run them under productive time and use engineering time when running recovery plates (goldens/monitors) after a down event. In our current use I would put engineering time inside of the down state window. I’m assuming your engineering time is more of the “recoverable” time, as from experimental lots?”

**Response from Jennifer:** Our green-to-green code classifies engineering time as a “green” state, meaning that it is treated like productive or standby time in terms of not being part of a green-to-green instance. We designate engineering time according to whatever is in SEMI E10. Or, in practice, whatever our customers log into the MES and then tell us to map into engineering time. My take is that any time the engineers are using the tool to run their own experiments, that’s engineering time. The tool is logged to an engineering state. If the production team is running a lot through the tool that is owned by the engineers, that time would usually count as productive time.



See more about Green-to-Green Charts in FabTime Newsletter 20.02, available to subscribers for download from the FabTime Newsletter Archive.

But I don't work directly on installation projects. I suspect there is some disagreement in general about this question. Therefore, I am including it here, to see if this will spark some discussion. Readers, do you think that experimental lots should be run under productive time or engineering time? If you have feedback, please [let me know](#). I will share responses in the next issue.

## The Waddington Effect: Responses to the Last Issue

A **longtime subscriber** wrote: "I never called it The Waddington Effect, but yes, I could see this happening. You're doing a triggered PM and you don't recover from the triggered PM and you can actually spend more time down than you planned on the flipside. You could be doing an unscheduled event and coupled with that pull in a PM activity and still have a bigger problem if you don't recover. The article focuses on the PM activity, turning into an unscheduled event, which happens quite frequently. However, I'm not sure that it's tied to the frequency of the PMs as much as the ability to properly execute the PM and recover and bring the system back up flawlessly."

A **subscriber who is an equipment engineering manager** wrote: "That's an interesting idea. I always had a feeling that there could be a connection between PMs and subsequent unscheduled downtimes. Now there's something worth investigating. I'll ask our improvement department to analyze this and will be curious to see your further results."

We welcome the opportunity to publish subscriber discussion questions and responses. [Submit your responses here](#).

## Main Article: Why and How Fabs Should Focus on CT Improvement

By Jennifer Robinson

As we start a new year, I thought it would be a good time to take a step back from the details and talk about why good cycle time matters for fabs, why it's difficult to achieve, and what we should do at a high level to improve it. If your management team doesn't believe that it's worth investing in cycle time improvement, or doesn't know how to get started, please consider passing along this issue.

### Why is cycle time improvement worthwhile financially?

There are three broad financial justifications for improving wafer fab cycle time:

1. Lower costs.
2. Higher prices.
3. Increased throughput.

#### 1. Lower Costs

There are two primary ways that cycle time improvement helps to





reduce costs: 1) by lowering the amount of WIP in the fab; and 2) by reducing scrap and rework.

**Lower WIP:** We know from Little's Law that if a fab retains the same throughput rate and reduces cycle time, WIP will also be reduced. (See Issue 21.06: Little's Law and Metrics Selection, available to subscribers for download from the FabTime Newsletter Archive). WIP reduction offers three opportunities for reducing costs:

- **ECN savings.** When there is less WIP in the fab, and an Engineering Change Notice is issued, fewer wafers will be affected. The cost savings can be estimated as  $\text{Change in WIP} \times \text{ECN \%} \times \text{Cost per wafer to address an ECN}$ .
- **Lower cost of carrying WIP.** Decreasing the WIP level in a fab results in a one-time reduction in the cost of carrying that WIP.
- **Less risk of writing off obsolete inventory (less safety stock required).** Whenever a fab holds inventory in post-fab, there's a possibility that some portion of that inventory will become obsolete before it can be sold. Having a shorter cycle time reduces the amount of inventory that must be held as safety stock and thus reduces the probability of that inventory being written off.

**Less Scrap and Rework:** Most people I talk with believe that shorter cycle times lead to fewer wafers scrapped. There's an intuitive argument that the less time a wafer spends in the fab, the less chance there is for something to go wrong. There's also the idea that if there's less WIP in the fab (as there will be if cycle times are reduced), then the fab team will learn about equipment problems sooner, such that fewer wafers will be impacted.

Better yields lead to reduced costs of:

- **Raw wafers** (we don't have to start as many wafers to achieve the same throughput).
- **Consumables** (we don't waste consumables on wafers that are eventually scrapped).

Similarly, having shorter cycle times probably correlates with doing less rework. As one example, the higher the WIP, the greater the chance of a time constraint between process steps being violated and triggering rework. (See [Issue 24.02: Managing Time Constraints between Process Steps in Wafer Fabs](#).) Doing less rework will also reduce consumables costs. See Issue 22.03 in our newsletter archive for more on the impact of rework on fab cycle time.

Having less scrap and rework frees up some wasted capacity on tools (capacity spent processing wafers that were later scrapped or re-processing rework). This helps to reduce cycle time further, leading to a positive feedback cycle.

## 2. High Prices from Reduced Time to Market

Increased sales revenue may be the most promising path in terms of justifying the cost of cycle time improvement efforts. It is also the path that is hardest to quantify, because it requires assumptions about what customers will pay in the future. However, as a very simple example, suppose that by reducing cycle time by 20%, your company can get a key new product to market more quickly, and can charge a 30% price premium (for some limited time). You can easily do the math to estimate what that might be worth for your company.

Here are three potential paths to increased sales revenue from shorter cycle time:

### **R1) Design Wins - Increased Cycles of Learning:**

Shorter R&D cycle times → More cycles of learning during product development → More time for experimentation and product refinement → More competitive products → Increased design wins → Increased revenue.

### **R2) Design Wins - First to Market:**

Shorter R&D cycle times → Faster product development → First to market → Increased design wins → Increased revenue.

### **R3) Pricing Premium - First to Market:**

Shorter R&D cycle times → More cycles of learning during product development → Faster product development → First to market → New product pricing premium → Increased revenue.

Of course, this matters more during certain parts of the market cycle and in certain market niches. But it is certainly true that shorter cycle time can correspond to higher revenue in many cases. If you work in a foundry, you may know exactly what the value of shorter cycle time is to your customers. See Volume 7, No. 7: Financial Justification for Cycle Time Improvement Efforts and Volume 3, No. 5: The Bottom-Line Benefits of Cycle Time Management, both available for download from the FabTime Newsletter Archive, for more details.

## **3. Increased Throughput**

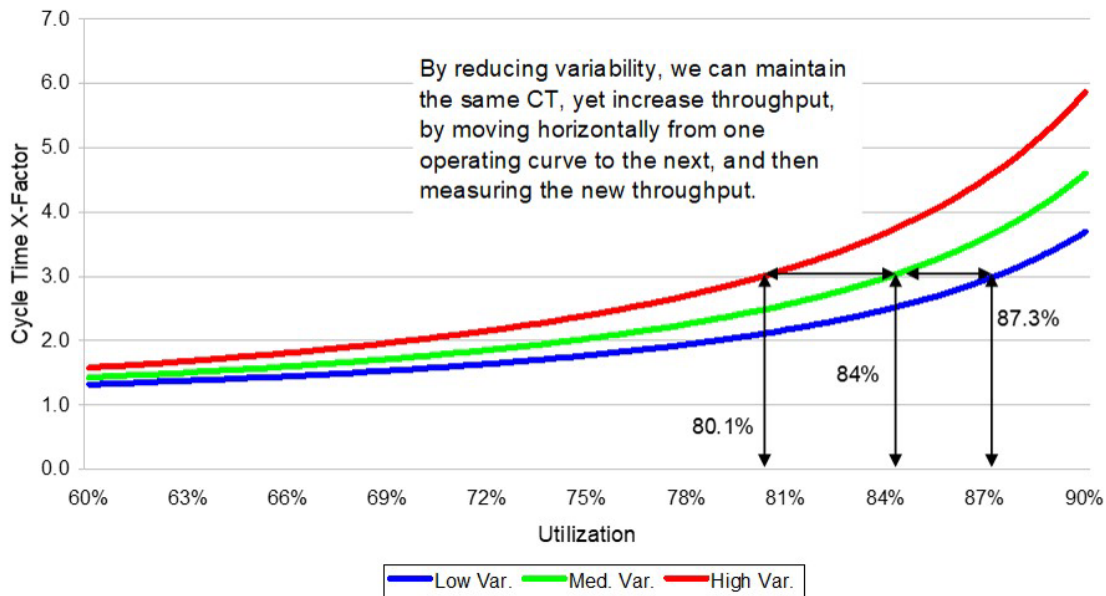
When industrial engineers plan capacity for a wafer fab, they plan to run each tool at some percentage of the time that the tool is available to manufacturing. As has been extensively discussed in this newsletter, it is typical to include a certain amount of buffer capacity for each tool, rather than planning to run the tools at 100% utilization. This buffer capacity helps the fab to recover from variability and avoids unacceptably high cycle times. The size of the buffer can vary depending on the number of like tools in a tool group, the cost of the tool, and other considerations. A typical buffer for tools with some redundancy is 15% of available time.

If a fab does a great job of reducing cycle time by reducing variability, it may be possible for that fab to reduce the buffer capacity on key tool groups. This allows the fab to flatten out the operating curve and achieve the target cycle time at a slightly higher loading of the tools. This means that for the same toolset and cycle time target, the fab can start additional wafers. If market conditions are such that the fab can sell the additional wafers, the financial benefit is easy to quantify (net profit per wafer times additional wafers produced over some time period).

An example is shown below. If this fab has a target average cycle time of 3X, and they are in the highest variability condition (the red curve), they'll have to limit the utilization of the bottleneck to 80.1%. Moving to a lower variability condition (the green curve) would allow them to increase bottleneck loading to 84%. Moving to the blue curve would allow that loading to increase to 87%. While the magnitude of this bottleneck utilization increase might be exaggerated, even a 1% or 2% increase in bottleneck loading (and hence in fab throughput) could be significant financially.



### 3x CT vs. Throughput Rate for High, Med, and Low Variability Fabs



### What other reasons are there to strive for good cycle times in the fab?

In the above section, we've explored several paths to reduced cost and/or increased revenue for a fab due to improved cycle time. Other benefits may be harder to quantify, but also add value. For example:

- **Shorter cycle times result in happier customers.** Shorter cycle times are usually also more predictable cycle times, resulting in better on-time delivery (OTD) performance. Better OTD performance makes customers happy.
- **Shorter cycle times result in happier managers.** A leaner fab with less WIP is more flexible and ready for market changes. A fab carrying less WIP is easier to manage in general.

Happier customers and happier employees. What's not to like about that?

### Given these many incentives, why don't fabs have better cycle time?

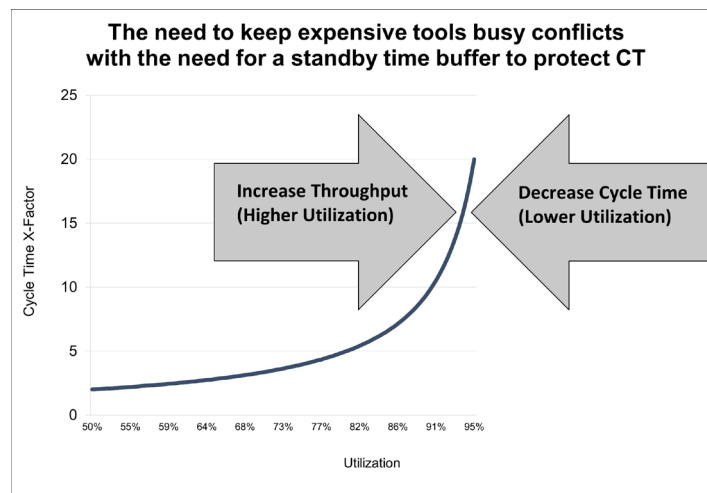
The short answer regarding why fabs don't have better cycle time is: **cost, complexity and change.**

- Wafer fab equipment is **expensive**.
  - A new cutting edge fab can cost up to \$20B.
  - The most expensive EUV tools cost \$200M each. Even "less expensive" legacy tools can cost \$5M to \$10M.
  - Fab managers are under pressure to keep these expensive tools busy! This results in high tool utilization (which we know drives high cycle times).
- Wafer fab process flows are **long** and **complex**. Products today can have close to 100 layers, and more than 1000 process steps. This introduces a LOT of variability, which, of course, increases cycle time.

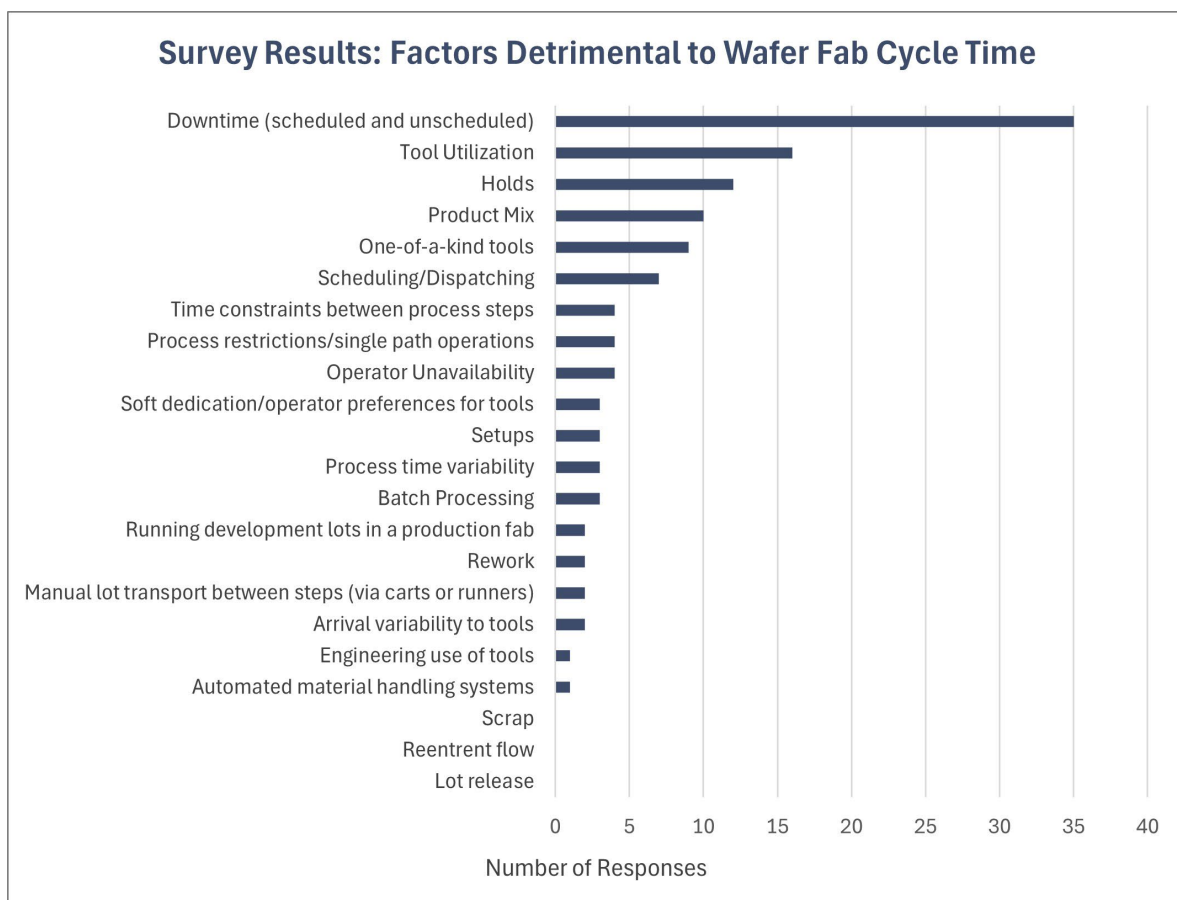
- Product and technology mix **change** rapidly. This means that:

- Process engineers may not be able to qualify new recipes on enough tools.
- Tools on the bleeding edge of technology may be unreliable because they're new.

- Legacy tools may be unreliable because they're worn out, and it's either technically infeasible or cost-prohibitive to replace them.



For 25 years, I've been asking people some variant of this question: "Why is cycle time high in your fab?" Respondents have cited many detailed reasons. For a year or so, we asked people who subscribed to this newsletter to choose what they believed to be the top contributor to fab cycle time from a list of options. Results from 123 respondents are aggregated below.



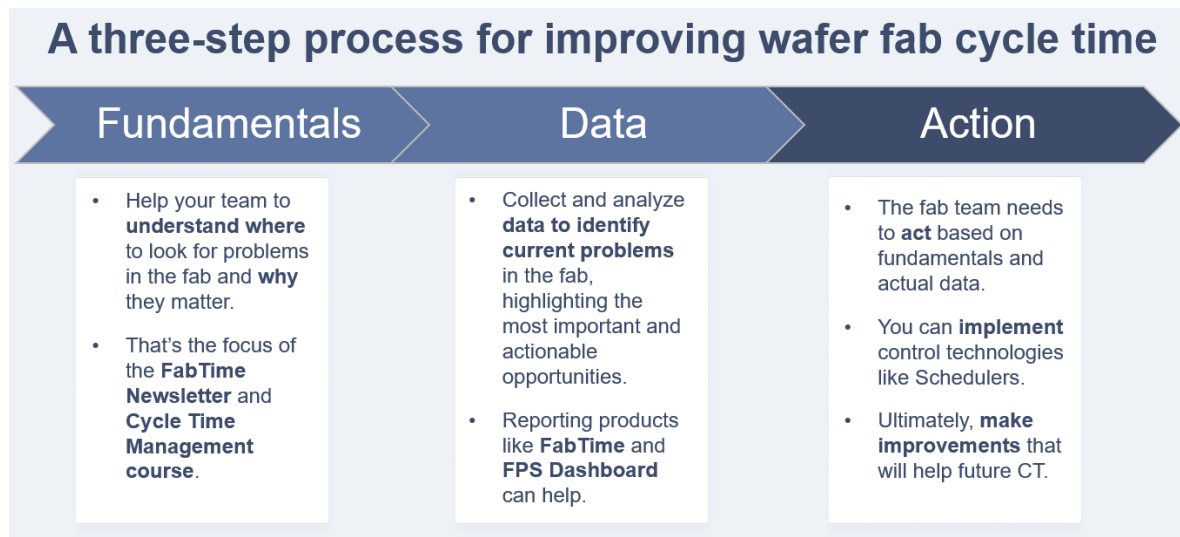
See [Issue 24.04: Commonly Reported Wafer Fab Cycle Time Contributors](#) for more information.

It's worth noting that some of the factors in the above list are fab-specific (time constraints between process steps, reentrant flow) while others apply to factories in general. What is undeniable is the fact that achieving great cycle time in a wafer fab is challenging (particularly when high demand is driving high utilization).

## So, what can you do? How should you begin if you want to improve cycle time in your fab?

We know that improving wafer fab cycle time is financially beneficial and helps make running the fab easier. The next question is: how should we go about it?

I propose a three-step process, as shown below.



**Fundamentals:** The first step is to help your team understand **where to look for problems and why**. That's the focus of this newsletter and our [cycle time class](#). If we don't understand how factories work, it's easy to make mistakes that degrade performance. These might include starting too many wafers, introducing too much variability, or letting a lack of operator or technician cross-training constrain your performance.

**Data:** The second thing that we need to improve fab cycle time is data. We need to be able to see and prioritize the **current problems in the fab** so that we can focus on the ones that offer the highest leverage. This data needs to be proactive. It's not enough to know what problems did occur (though there can be valuable learning in that). We want to know what problems we can tackle today that will help us to improve cycle time in the future.

**Action:** We can spend as much time as we like learning about factory physics and collecting data about what's going on in the fab. If we don't take any action, we will not see any improvement. Actions to take may include:

- Purchasing tools and hiring people.
- Making operational changes (batch tools, PM schedules, etc.) to reduce variability or free up buffer capacity.

- Implementing control technologies like schedulers and other [Smart Manufacturing solutions](#).

What matters is taking some form of action. Ideally, we can measure performance before and after acting, to see what works best in a given fab.

## What resources are available to help?

**Fundamentals:** Several resources for understanding fab cycle time fundamentals are available from the INFICON website, including:

- Past issues of the FabTime Newsletter in PDF format. Subscribers can download individual issues or a full archive. There is also a PDF file containing the abstracts from all newsletter issues to date. You can find the archive link in any newsletter email or [reach out to Jennifer](#).
- The [FabTime Operating Curve Spreadsheet](#), a useful Excel-based tool for exploring tradeoffs related to variability, utilization, and number of qualified tools.
- Information about the [FabTime Cycle Time Management Course](#), a four-hour Teams-based course to help your team to understand the fundamental drivers of wafer fab cycle time.
- [A PDF file containing a tutorial on wafer fab cycle time](#) as well as various queueing formulas, created back in the early days of FabTime.
- A video of my FOA Fab Star Webinar on the fundamental drivers of fab cycle time. [Follow this link](#) and scroll to the bottom of the page to watch.

**Data:** The INFICON [FabTime](#) and [Factory Dashboard](#) software products were both designed to give people who work in wafer fabs access to the data they need to make improvements. Examples include:

- Operation cycle time data by tool group, as well as hours of WIP waiting for each tool group. Both of these charts highlight the tools that are contributing the most to cycle time right now. Making improvements at these tools can improve future cycle time.
- Dynamic cycle time and dynamic x-factor, which both give a forward look at cycle time, so that problems can be corrected now, before lots ship late.
- Standby-WIP-waiting time and post-process time by tool group, which can be an indicator of staffing constraints.
- Current equipment status and upcoming scheduled maintenance, so that engineers can be deployed appropriately.

**Action:** One way to take action towards cycle time improvement is to add capacity and/or staff. This approach is not always feasible, of course. However, there are many actions that you can take to reduce variability in your fab, and to make the fab run more effectively. These actions include changing operating practices and using smarter software tools.

- Several articles from the FabTime Newsletter feature suggestions for changes in operating practices, including:
  - [A Fab Cycle Time Improvement Framework \(Issue 23.06\)](#)
  - [10 Recommendations for Fab Cycle Time Improvement \(Issue 22.02\)](#)

- [10 More Recommendations for Improving Fab Cycle Time \(Issue 24.01\)](#)
- Many fabs are moving from standard dispatching to smart scheduling. The INFICON [Factory Scheduler](#) uses advanced heuristics, linear programming, optimization, and intelligent search algorithms to generate real-time optimized schedules for your fab. The integrated [NextMove](#) product provides direction to material handlers and operators on the floor.

## Conclusions

There are clear financial and qualitative benefits to reducing wafer fab cycle time, although structural realities in the fab environment make this difficult. Expensive tools, complex process flows, and high levels of product mix result in high utilization and variability and insufficient tool redundancy. We believe that a three-pronged approach is necessary to improve fab cycle times. Fab teams need education to understand where to look for problems and why. They also need flexible access to data that highlights both current and future problems. Finally, they need to act, whether by expanding capacity and staffing, making changes to operating practices, or adding software control technologies. We've included links to resources that we offer in these areas and look forward to the opportunity to help.

## Acknowledgements

Thank you to the many individuals who have actively participated in sessions of our cycle time management class. We learn something new from every group, and that increasing knowledge base has informed this article.

# Subscriber List

**Total number of subscribers: 2,799**

## **Top 20 subscribing companies:**

- onsemi (123)
- Micron Technology (113)
- Intel (112)
- Infineon (106)
- Microchip Technology (101)
- Analog Devices (98)
- Skyworks Solutions (92)
- GlobalFoundries (77)
- NXP (70)
- STMicroelectronics (67)
- Texas Instruments (66)
- Seagate Technology (57)
- X-FAB (56)
- Western Digital (55)
- Wolfspeed (52)
- Tower Semiconductor (37)
- Applied Materials (36)
- Qualcomm (36)
- ASML (33)
- SkyWater Technology (30)

## **Top 4 subscribing universities:**

- Arizona State University (7)
- Ben Gurion University of the Negev (5)
- Ecole des Mines de St. Etienne (EMSE) (3)
- Nanyang Technological University (3)

**Note:** Inclusion in the subscriber profile for this newsletter indicates an interest, on the part of individual subscribers, in cycle time management. It does not imply any endorsement of INFICON or its products by any individual or his or her company.

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